In the Claims

1. (Currently Amended) A liquid crystal display, comprising:

a plurality of first, second, and third gate lines transmitting scanning signals provided on first, second, and third areas, respectively, wherein one of the first gate lines and one of the third gate lines are simultaneously scanned and the second gate lines are scanned after the first and the third gate lines;

a plurality of pairs of first and second data lines transmitting data voltages, each pair of first and second data lines separated from each other at a disconnection; and

a plurality of pixels connected to the gate lines and the data lines, arranged in a matrix, and including a plurality of first, second, and third pixels provided on the first, the second, and the third areas, respectively,

wherein the disconnections of the first and the second data lines are randomly distributed on the second area.

2. (Canceled)

3. (Original) The liquid crystal display of claim 1, wherein each pair of first and second data lines are supplied with a single data voltage during the scanning of each of the second gate lines.

4. (Original) The liquid crystal display of claim 1, wherein the number of the first gate lines is equal to the number of the third gate lines, and the second area is disposed between the first area and the third area.

5. (Original) The liquid crystal display of claim 4, wherein the scanning directions for the first, the second, and the third gate lines are the same.

6. (Original) The liquid crystal display of claim 1, further comprising:

first and second data drivers applying the data voltages to the first and the second data lines, respectively;

a gate driver applying the scanning signals to the first, the second, and the third gate lines; and

a memory storing image data corresponding to the data voltages and supplying the image data to the first and the second data drivers.

7. (Original) The liquid crystal display of claim 6, wherein the image data are written in the memory in synchronization with a write clock and are read in synchronization with a read clock having a frequency substantially half of a frequency of the write clock.

8. (Original) The liquid crystal display of claim 6, wherein the image data for the first pixels and the third pixels are supplied to the first data driver and the second data driver, respectively, and the image data for the second pixels are supplied to both the first and the second data drivers.

9. (Canceled)

10. (Original) The liquid crystal display of claim 6, wherein the number of the first gate lines is equal to the number of the third gate lines, and the second area is disposed between the first area and the third area.

11. (Original) The liquid crystal display of claim 10, wherein the scanning directions for the first, the second, and the third gate lines are the same.

12. (Original) A method of driving a liquid crystal display including a plurality of first, second, and third gate lines transmitting scanning signals provided on first, second, and third areas, respectively, a plurality of pairs of first and second data lines transmitting data voltages and separated from each other at a plurality of disconnections randomly distributed on the second area, and a plurality of pixels connected to the gate lines and the data lines and including a plurality of first, second, and third pixels provided on the first, the second, and the third areas, respectively, the

method comprising:

sequentially applying scanning signals to the first gate lines and the third gate lines in pairs at the same time;

applying data voltages for the first pixels and the third pixels to the first data lines and the second data lines, respectively;

sequentially applying scanning signals to the second gate lines; and

applying data voltages for the second pixels to both the first and the second data lines.

13. (Original) The method of claim 12, wherein the application of scanning signals to the second gate lines is performed after the application of scanning signals to the first gate lines and the third gate lines.

14. (Original) The method of claim 12, further comprising:

writing image signals corresponding to the data voltages into a memory in synchronization with a write clock;

reading out the image signals for the first and the third pixels in synchronization with a read clock;

converting the read-out image signals for the first and the third pixels into the data voltages;

reading out the image signals for the second pixels in synchronization with the read clock; and

converting the read-out image signals for the second pixels into the data voltages.

15. (Original) The method of claim 14, wherein the read clock has a frequency substantially equal to half of a frequency of the write clock.